EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _

Exam 2
Fall 2020 (Oct 9 2020)

Instructions: There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam, on separate sheets of white paper, or on a tablet pc. When finished, scan or image and upload as a .pdf file on Canvas. Exams are due by 1:00 p.m.

Due to the online nature of this exam, students will be expected to adhere to the honor system and acknowledge adherence with a signature given below. This is an open-book open-notes exam and students can seek basic information using online resources but with the following absolute restrictions. Prior to the Canvas upload due time, no questions or problems should be posted on any electronic forum, no discussions are permitted relating to this exam with anyone else besides the course instructor, and no solutions obtained from any source other than by the student taking the exam is permitted. The course instructor will attempt to respond to questions by email that are sent between 11:00 a.m. and 1:00 p.m.

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}$=100µA/V^2 ,$\mu_p C_{OX}=\mu_n C_{OX}/3$,V_{TNO}=0.5V, V_{TPO}= - 0.5V, C_{OX}=8fF/µ^2, $\lambda = 0$. Correspondingly, assume all npn BJT transistors have model parameters J_S= 10^{-14}A/µ^2 and β=100 and all pnp BJT transistors have model parameters J_S= 10^{-14}A/µ^2 and $\beta = 25$. If the emitter area of a transistor is not given, assume it is 100µ^2 . If reference to a diode is made, assume the process parameter J_S=10^{-17}A/µ^2 , V_{G0}=1.17V, and m=2.3. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E- 5 V/K. If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

Honor System Adherence Signature:

I certify that I have adhered to the honor system policy described in the second paragraph above ___________________

Short Questions

1. (2 pts) How many model parameters are there in a 16-bin binning model if each bin used a BSIM device model?

2. (2 pts) One of the models that was introduced for the MOS transistor was the α-law model. Though it is more accurate than the square-law model for very small transistors, it is not used much. Why is the α-law model not used much?

3. (2pts) Why is the β of the vertical transistor typically much larger than the β of a lateral transistor in a typical bipolar process?

4. (2 pts) Why is CVD used instead of thermal growth when placing a SiO_2 layer on top of an aluminum interconnect?

5 (2 pts) True or False: When operating in the forward active region the BE junction of a BJT is forward biased and the BC junction is forward biased for npn transistors?

6. (2pts) What parameter in the model of the BJT models the slope of the output characteristics in the Forward Active region?

7. (2pts) Why is an epitaxial process used to create the collector region of a BJT instead of an n-type diffusion in a typical bipolar process?

8. (2pts) The term "increasing the power of a signal" is commonly used when describing an electronic amplifier. The input and output signals in an amplifier are, however, often voltages. What does it mean to "increase the power of a signal?" when the signals of interest are voltages?

9. (2pts) Through the 50's and 60's, bipolar processes were exclusively used to build integrated circuits with active devices. Why were the CMOS processes that are widely used today not used in the 50's and 60's?

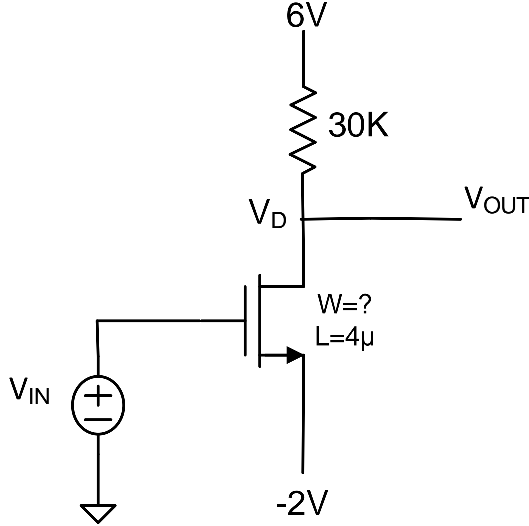
10. (2pts) Why are designers not able to make a direct contact between Metal 2 and active in the standard CMOS process flow that was discussed in class?

Problems

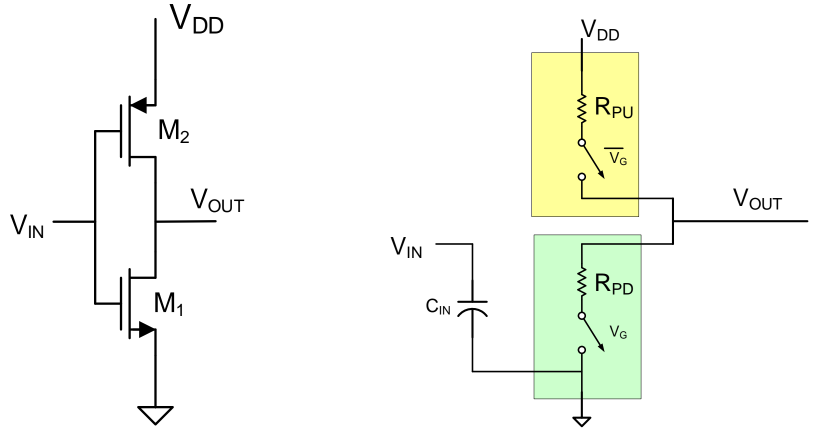
Problem 1 (16 pt) Consider the following circuit.

a) Determine W so that the quiescent output voltage is 0V

b) If V_{IN}=0.02sin(100t), determine the output voltage with the value of W determined in part a)

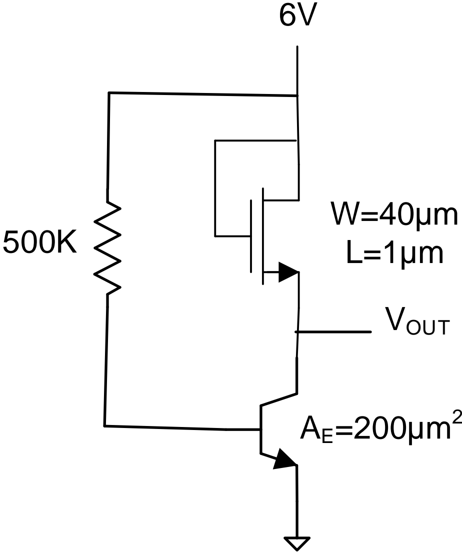


Problem 2 A switch-level model for a digital inverter is shown below. If the supply voltage is 2.2V, determine the parameters in the switch-level model if the inverter is designed in the 0.18um process (model information attached to this exam) with dimensions L_1=L_2=0.5µm and W_1=W_2=4µm.



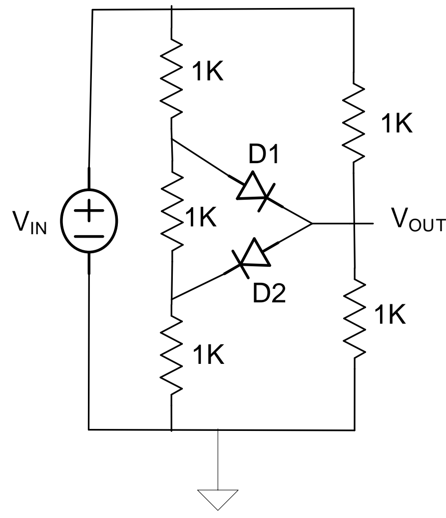
Problem 3

Determine V_{OUT}. Assume the bipolar transistor has parameters β=100 and $J_S=10^{-14}A/\mu^2$ and the MOS transistor has parameters $uC_{OX}=100\mu A/V^2$ and V_{TH}=1V.



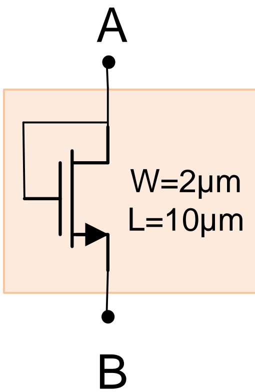
Problem 4 (16 pts) Consider the following circuit where the diodes are assumed to be modeled by the equation
$$\begin{cases} I_D = 0 & \text{if } V_D < 0.6V \\ V_D = 0.6V & \text{if } I_D > 0 \end{cases}$$

a) Determine V_{OUT} if V_{IN} =3V
b) For 0<t<6, obtain an expression for and plot V_{OUT} if V_{IN}=6t
c) Extra Credit (8 pts) Obtain an expression for and plot $V_{OUT}(t)$ if $V_{IN}(t)$=6sin(10t) for one period of the input.



Problem 5 (16 pts) Consider the following one-port where the MOS transistor has parameters V_{TN}=0.5V $\mu_n C_{OX}$=300µAV^{-2} and λ=0. Assume the quiescent current was measured to be I_Q=4mA.

a) Determine the quiescent voltage between nodes A and B
b) The small-signal equivalent circuit of any one-port at any Q-point is a resistor. Derive the small-signal equivalent of the one-port between nodes A and B at the Q-point specified.



MOSIS WAFER ACCEPTANCE TESTS

RUN: T68B (MM_NON-EPI) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.51	volts
SHORT	20.0/0.18			
Idss		547	-250	uA/um
Vth		0.51	-0.51	volts
Vpt		4.8	-5.6	volts
WIDE	20.0/0.18			
Ids0		14.4	-4.7	pA/um
LARGE	50/50			
Vth		0.43	-0.42	volts
Vjbkd		3.1	-4.3	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		175.4	-35.6	uA/V^2
Low-field Mobility		416.52	84.54	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology		XL (um)	XW um)
SCN6M_DEEP (lambda=0.09)		0.00	-0.01
	thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)		-0.02	0.00
	thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.7	7.8	8.0	59.7	313.6	0.08	0.08	ohms/sq
Contact Resistance	10.6	11.0	10.0				4.79	ohms
Gate Oxide Thickness	41							angstrom

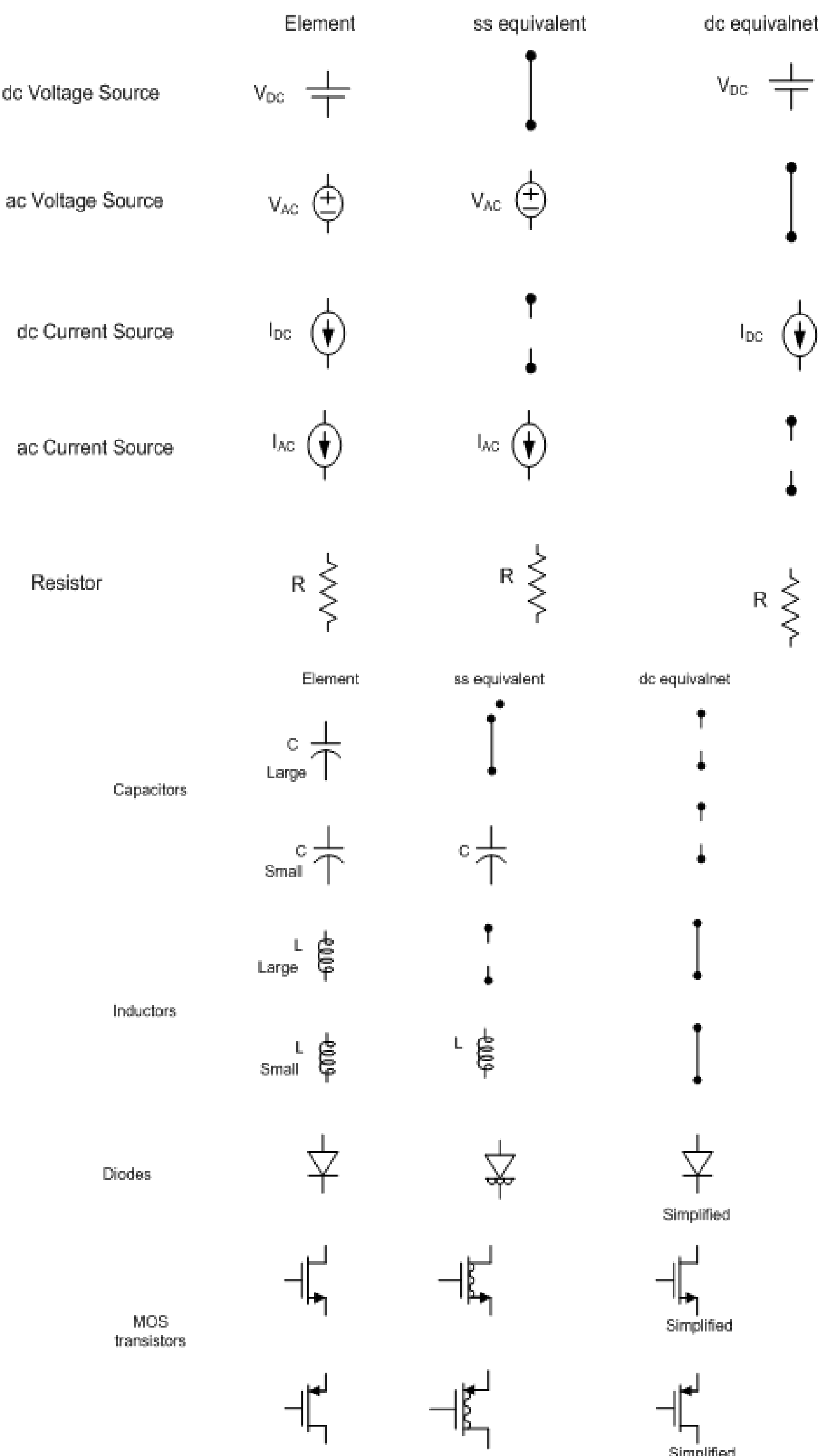
PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08		0.08	0.08	0.03	930	ohms/sq
Contact Resistance	9.24		14.05	18.39	20.69		ohms

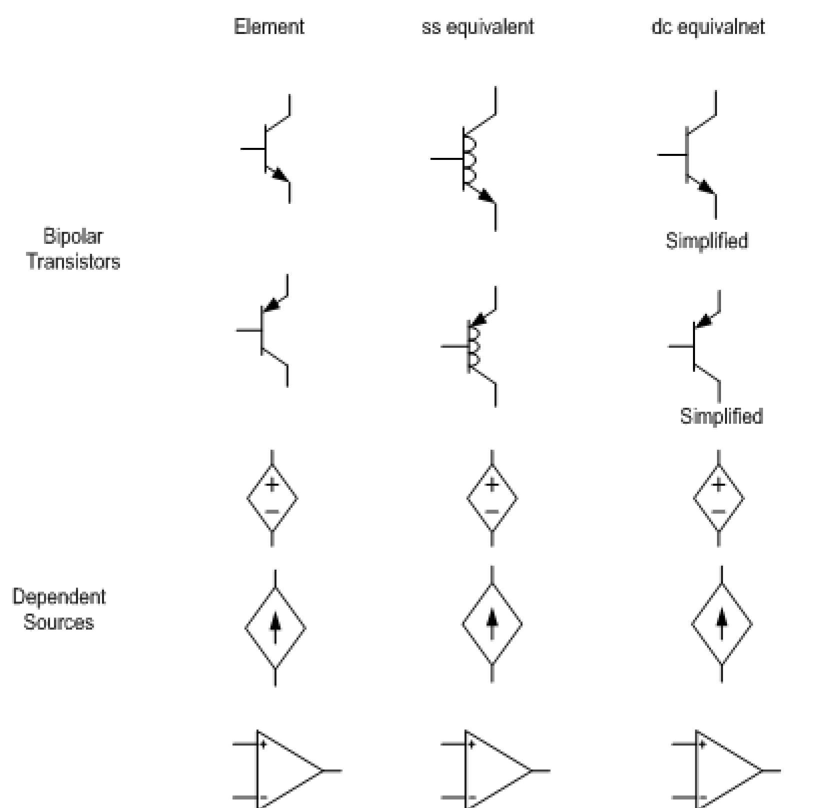
COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34			984		aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235		41	35	29	21	14						aF/um
Fringe (poly)				70	39	29	23	20	17					aF/um
Fringe (metal1)					52	34		22	19					aF/um
Fringe (metal2)						48	35	27	22					aF/um
Fringe (metal3)							53	34	27					aF/um
Fringe (metal4)								58	35					aF/um
Fringe (metal5)									55					aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.72	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		300.36	MHz
DIV1024 (31-stg,1.8V)		363.77	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Bipolar
Transistors
Simplified
Simplified
Dependent
Sources